IN THE CLAIMS

Please amend claim 21 as indicated below.

This listing of claims will replace all prior versions, and listings, of the claims in the Application.

Listing of Claims:

Claim 1 (previously presented) A flash memory device comprising:

a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;

at least one component including a polysilicon layer having a top surface, wherein the at least one component is formed on a field oxide region configured to separate the plurality of gate stacks;

a silicide on the top surface of the polysilicon layer of the at least one component; and

an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein.

Claim 2 (original) The flash memory device of claim 1 wherein the silicide further includes a titanium silicide.

Claim 3 (original) The flash memory device of claim 1 wherein the silicide further includes a cobalt silicide.

Claims 4-7 (cancelled)

Claim 8 (withdrawn) A method for providing at least one contact in a flash memory device, the flash memory device including a plurality of gate stacks and at least one component including a polysilicon layer having a top surface, the method comprising the steps of:

(a) forming a silicide on the top surface of the polysilicon layer;

(b) providing an insulating layer covering the plurality of gate stacks, the at least one component and the silicide;

(c) etching the insulating layer to provide at least one contact hole, the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer;

(d) filling the at least one contact hole with a conductor.

Claim 9 (withdrawn) The method of claim 8 wherein the at least one contact hole further includes a plurality of contact holes, wherein a plurality of source/drain regions are adjacent to the plurality of gate stacks, and wherein the insulating layer etching step (c) further includes the steps of:

(c1) etching the insulating layer to expose a portion of the plurality of gate stacks in a first portion of the plurality of contact holes, to expose a portion of the plurality of source/drain regions in a second portion of the plurality of contact holes and to expose the silicide on the at least one polysilicon device in a third portion of the plurality of contact holes.

Claim 10 (withdrawn) The method of claim 8 wherein the silicide further includes a titanium silicide.

Claim 11 (withdrawn) The method of claim 8 wherein the silicide further includes a cobalt silicide.

Claim 12 (withdrawn) The method of claim 8 wherein the component further includes an oxide-nitride-oxide layer on the polysilicon layer and wherein the method further includes the step of:

(e) removing the oxide-nitride-oxide layer prior to formation of the silicide.

Claim 13 (withdrawn) The method of claim 12 wherein the oxide-nitride-oxide layer removing step (e) further includes the step of:

(e1) removing the oxide-nitride-oxide layer during a polysilicon layer etching

step which forms the plurality of gate stacks.

Claim 14 (withdrawn) The method of claim 12 wherein the plurality of gate stacks further include a plurality of spacers and wherein the oxide-nitride-oxide layer removing step (e) further includes the step of:

(e1) removing the oxide-nitride-oxide layer after formation of the plurality of spacers.

Claim 15 (withdrawn) The method of claim 8 wherein the flash memory device further includes at least one field oxide region, the at least one component being located on the at least one field oxide region.

Claim 16 (withdrawn) The method of claim 8 wherein the silicide forming step (a) further includes the step of:

(a1) using a self-aligned silicide process to form the silicide on the top surface of the polysilicon layer.

Claim 17 (previously presented) A flash memory device, comprising:

an oxide layer;

a gate stack formed on said oxide layer, wherein said gate stack comprises:

a first polysilicon layer;

an insulating layer formed on said first polysilicon layer; and

a second polysilicon layer formed on said insulating layer;

a field oxide region located adjacent to said oxide layer;

a component located on said field oxide region, wherein said component is formed from one of said first and said second polysilicon layer; and

a silicide layer formed on said component.

Claim 18 (previously presented) The flash memory device as recited in claim 17, wherein said silicide layer on said component prevents etching through one of said first and said second polysilicon layer.

Claim 19 (previously presented) The flash memory device as recited in claim 17, wherein said silicide layer comprises a titanium silicide.

Claim 20 (previously presented) The flash memory device as recited in claim 17, wherein said silicide layer comprises a cobalt silicide.

Claim 21 (currently amended) ~~The flash memory device as recited in claim 17,~~ A flash memory device, comprising:

an oxide layer;

a gate stack formed on said oxide layer, wherein said gate stack comprises:

a first polysilicon layer;

an insulating layer formed on said first polysilicon layer; and

a second polysilicon layer formed on said insulating layer;

a field oxide region located adjacent to said oxide layer;

a component located on said field oxide region, wherein said component is formed from one of said first and said second polysilicon layer; and

a silicide layer formed on said component;

wherein said component comprises a resistor.